of this amendment and reconsideration to that end is respectfully requested.

Claims 1-3 have been finally rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,061,766, issued to Lynch et al (hereinafter referred to as "Lynch"). This ground of rejection is respectfully traversed as to claims 1-3 for the following reasons.

Claim 1 is limited by a "level two cache memory" coupled to a "level three cache memory" by a "system bus" wherein the system bus is monitored by a "SNOOP circuit". Lynch does not have this configuration so it cannot anticipate claim 1.

Lynch has no "level three cache memory". This was pointed out to the Examiner in Applicant's previous submission. In response thereto, the Examiner states:

> As is well know (sic) in the art, it is customary in a cache hierarchy comprising three levels to use the main memory as the upper level cache or L3 cache. Examiner would like to point applicant's attention to Fig. 1 and 2 of the Fletcher et al (4,442,487) reference submitted as IDS on December 18, 2000 where such a configuration is used. The cache hierarchy is nothing more than a small, high speed memory unit used to improve the performance of a CPU. <u>The higher the cache level, the slower the access as the memory capacity increases.</u> (Emphasis added)

Thus, quite apart from the inaccuracy of the emphasized portion of the Examiner's argument, even more important is that the Examiner admits that Lynch does not teach a "third level cache memory" as previously asserted by Applicant. It is not clear

from this argument whether the Examiner wishes to suggest that his rejection is based upon "inherency" (i.e., all main memories must inherently have a level three cache memory). However, it is readily apparent that the Examiner has not even attempted to meet his burden of proof of inherency required by MPEP 2112. It is also readily apparent that he could not do so, because the prior art is replete with main memories which do not incorporate a level three cache memory.

Applicant has asserted that Lynch does not show a "system bus". Both Lynch (see col. 3, lines 37-38) and the Examiner agree that this is so. Though Lynch mentions a "common memory bus (not shown)", it is important that the reference says nothing more about it. That means that Lynch does not "SNOOP" the "common memory bus". Lynch has no circuit for SNOOPing the system bus as is limiting of Applicant's invention. The SNOOP functions of Lynch are performed within System Interface Unit (SIU) 312. As can be readily seen from Fig. 3 of Lynch, SIU 312 is located within CPU 302 between D$ 308/I$ 310 and E$ 306.

In accordance with the Examiner's reading of Lynch, that means that the SNOOP circuit of Lynch operates between level one and level two cache memories rather than between level two and level three cache memories as is limiting of Applicant's claims. This distinction is not trivial, because Lynch teaches and requires that all processors must interface with SIU 312 (i.e., a

single level two cache memory). In Applicant's system, SNOOPing the system bus permits each processor to have dedicated level two cache memories as taught, for example, at page 6, lines 21-23, of the specification.

Claim 2 depends from claim 1 and is further limited by "second logic which inhibits said first logic from invalidating for mode 3 requests without ownership". Applicant has previously pointed out why Lynch does not teach or suggest this limitation. In response, the Examiner states:

> Examiner would like to point out that the snoop requests of Lynch indicates the snooping of level three caches since the Lynch reference indicates the presence or absence of the snooped data object in each cache as detailed in column 4, lines 30-32. (Emphasis added)

Clearly, Lynch does not show "snooping of level three caches". This is explained in detail below. Furthermore, column 4, lines 30-32, states:

> The lines 316 and 318 are preferably one-bit wide, indicating the presence or absence of the snooped data object in each cache.

Lines 316 and 318 are located **within** CPU 302. The Examiner fails to even allege how these lines are possibly coupled to the alleged level three cache memory (not shown).

Claim 3 depends from claim 2 and is further limited by "third logic which invalidates said corresponding cache memory location in response to a SNOOP hit". Applicant argued in his previous submission that the Examiner had impermissibly read the

claimed "second logic" and "third logic" structures on to a single structure of Lynch. Confusingly, the Examiner responded by stating:

> Considering that logic steps are used as aids in showing the way a proposed program will work and that each step processes information by performing a logical operation on it, it is clearly obvious that any computer system uses a combination of logics to produce outputs based on the rules of logic it is designed to follow. Thus, multiple logics must be used as part of the system to obtain desired results.

Thus, it is not clear whether the Examiner has again relied upon "inherency" without making the showings required by MPEP 2112, or has instead decided that the proper rejection of claim 3 is more appropriately based upon 35 U.S.C. 103(a). In either event, it is apparent that the Examiner no longer considers the current anticipation rejection to be appropriate.

Claim 4 depends from claim 3 and is further limited by "fourth logic which retrieves and records data in response to a level one cache memory read miss and a level two cache memory read miss". Applicant has previously argued that Lynch does not meet this limitation. Apparently, the Examiner agrees, but inexplicably continues his anticipation rejection, stating:

> Examiner agrees with applicant that the portion cited by Examiner does not teach a step that "retrieves or records data". However, Examiner would like to point out that a snoop request is issued when a processor desires exclusive use of an object from main memory as detailed on page 3, column 56-58 (sic). Therefore, the processor must retrieve the object from main memory for its exclusive use as is well known in the art. Further, the system cannot afford to waste resources in

> performing snoops if it was not for the purpose of retrieving or storing data.

The Examiner may have confused "retrieving and recording a level two cache memory read miss" with retrieving and storing data from memory. In any event, it is apparent that the Examiner admits that the anticipation rejection of claim 4 is inappropriate.

Claim 5 depends from claim 4 and is further limited by "a fifth logic element". The Examiner has previously rejected this claim under 35 U.S.C. 103(a) as being rendered unpatentable over an alleged combination. Applicant has previously pointed out that the Examiner's rejection has failed to make a *prima facie* case of obviousness as specified by MPEP 2143 which requires a showing of "motivation", "reasonable likelihood of success", and "all claimed elements". Specifically, Applicant has shown that the Examiner has evidenced none of these in his rejection of claim 5. Instead of providing the required evidence, the Examiner reiterates that his findings are merely conclusory. He states:

> In this case, the conclusion and motivation is (sic) extracted directly from the reference of record. Therefore, the motivation is proper.

Though the Examiner concludes that his "conclusion and motivation" are "extracted directly from the reference of record", he does not specify which reference or where within that reference.

Claim 6 has been finally rejected as anticipated by U.S. Patent No. 6,397,300, issued to Arimilli et al (hereinafter referred to as "Arimilli"). Applicant has previously pointed out that Arimilli has neither a "system bus" nor a "level three cache" as is limiting of the claimed invention.

Unlike Lynch which does not disclose a level three cache memory, Arimilli specifically disclaims it. Arimilli states at column 8, lines 33-35:

> ....a multi-level cache hierarchy comprised of an upper, or L1 cache 200, and a lower, or L2 cache 202.

Arimilli takes pains to limit its disclosure to a two level cache memroy hierarchy. The Examiner does not even bother to allege that Arimilli has a "system bus".

Claim 6 is further limited by "first circuit which invalidates a corresponding portion of said level one cache memory in response to a level one cache memory write hit and a level two cache memory write". In other words, unlike Arimilli, the invention invalidation results from the coincidence of "a level one cache memory write hit" and "a level two cache memory write". Applicant has previously pointed this out to the Examiner. Misreading the claim, the Examiner states:

> In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "simultaneous write") are not recited in the rejected claim(s).

It is asserted that a proper reading of claim 6 and Arimilli would compel a finding of non-anticipation.

Claims 7-9, which depend from claim 6, have been finally rejected under 35 U.S.C. 103(a) over Arimilli in view of Lynch. Applicant has previously pointed out why the Examiner has failed to make a *prima facie* case of obviousness. The Examiner has neither provided the evidence required by MPEP 2143, nor indicated why such a showing should not required.

Claim 10 stands finally rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli in view of Hazawa. In addition to the Examiner's failure to make the *prima facie* case of obviousness, as previously detailed by Applicant, the Examiner has admitted that this rejection is inadequate, as a matter of law. Claim 10 depends from claim 6, and therefore contains all of the limitations of claim 6. Yet, the Examiner admits that Arimilli does not have all of the limitations of claim 6:

> Arimilli does not specifically teach a second logic which inhibits said first logic from invalidating for mode 3 requests without ownership.

Thus, the alleged combination of Arimilli and Hazawa does not meet all of the limitations of claim 10 (which necessarily includes all of the limitations of claim 6), as admitted by the Examiner.

In making his rejection of claims 11-15 and 16-20, the Examiner admits the legal inadequacy of his rejections. He states:

> Claim 16 is directed to the same invention as claim 11 and, as such does not require a different or separate base (sic) or rejection.

Claims 16-20 contain only "means-plus-function" limitations. Therefore, MPEP 2182, et seq. specifically requires a different level of examination.

Having thus responded to each objection and ground of rejection, Applicants respectfully request entry of this amendment and allowance of claims 1-20, being the only pending claims.

Respectfully submitted,

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By his attorney,

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